# Taurus: An Intelligent Data Plane

#### Problem Statement Approaches to managing datacenter networks are either: Slow but intelligent Fast yet dumb (e.g., anomaly detection) (e.g., ECMP) Intelligence (Controller) Data Plane (Switch or NIC) Data Plane (Switch or NIC) Can we get *fast and intelligent* approaches by moving the intelligence into the data plane? Packet Data Plane Packet Intelligence (Switch or NIC) Out In Data Plane Expressiveness • Popular networking DSLs like P4 already Data In comprise of multiple programming abstractions. • However, none of these are suitable for machine learning tasks. • We propose adding a new abstraction for machine intelligence: Map-Reduce.

Abstraction	Implementation		Par
Parsing	FSMs:		
Match-Action	RMT+VLIW:		• The
Scheduling	PIFO:		• We
Map-Reduce (Intelligence)	Parallel Patterns		- arci • Tau _ 12

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## Design of Taurus

We design our hardware around the **Map-Reduce** pattern to support machine intelligence and exploit inherent parallelism for high throughput and low latency execution of learned algorithms.

#### Architecture

- A Map-Reduce compute unit consists of:
- 1. Pipelined SIMD lanes of functional units (FU) and pipeline registers (PR).
- 2. A reduction network ...



Compute Units (**CU**) are interspersed with scratchpad memory units (MU) to exploit data locality.



#### Taurus Pipeline



- e Map-Reduce engine is embedded between tch-action tables in the ingress pipeline.
- prototype Taurus using the **Plasticine** chitecture and **Spatial** HDL.

urus's peak throughput ranges from 512 Gbps 12 Tbps depending on packet and model sizes.

### Taurus in the Datacenter

Datacenter operators can run Taurus both inside the network switches as well as at the end-host NICs.

## —— Taurus in Switches ——

- network.
- Enables intelligent applications like anomaly detection, routing, and load **balancing** using learned functions that operate at line rate.



# —— Taurus in Hosts' NICs -

- (Indigo) and RSS (Shenango).



• High throughput allows switches to apply learned functions to every packet in the

• Taurus can implement end-host functions for applications like **congestion control** 

Learned algorithms with feedback allows for smarter core and packet scheduling.



## Evaluation

## Microbenchmarks

Latency across different microbenchmarks:



Unrolling factors required to hit 1 GPkt/s:



# App. Benchmarks

Overheads are calculated relative to a 300 mm<sup>2</sup> chip with 4 pipelines each drawing an estimated 25 W.

#### Anomaly Detection:

The models are fully unrolled to meet typical switch line rates (512 Gbps – 12 Tbps).

		Area		Р
Model	Lat (ns)	$\mathrm{mm}^2$	+%	mW
SVM	68	4.59	6.1	263
DNN	362	8.80	11.7	506

Indigo Congestion Control  $\bullet$ 

The model is unrolled to meet typical NIC line rates (40 Gbps – 96 Gbps).

		Area		P
Model	Lat (ns)	$\mathrm{mm}^2$	+%	mW
LSTM	380	17.73	23.6	1018

CPU Cores



























